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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/810,005	03/16/2001	Zhongze Wang	303.747US1	7517

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/810,005	Applicant(s) WANG ET AL.	
	Examiner Samuel A Gebremariam	Art Unit 2811	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48 and 54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48 and 54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-48 and 54 drawn to a method of making semiconductor device in Paper No. 6 is acknowledged.

2. Applicant's cancellation without traverse of group I, claims 49-53 drawn to a semiconductor device in Paper No. 6 is acknowledged.

Specification

3. The disclosure is objected to because of the following informalities:

page 2, third paragraph call attention to reference figure "520", which does not exist in the drawings. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 4, 5, 9, 10, 16, 17, 23, 24, 31, 32, 37, 38, 44 and 45, are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not clear how a dielectric layer can be turned into a silicon nitride layer by remote plasma nitride processing. In this particular case it is not clear how by nitride processing a silicon oxide layer, a silicon nitride layer is formed. It is not clear how composite oxidation processing of the gate dielectric turn the gate dielectric layer to a silicon nitride layer either. It is

widely known that one can possibly form oxynitride layer by the process discussed above.

Claims 35-48, are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not clear how a number of word lines are coupled to the gates of the number of transistors. Applicants use of the word "coupled" is not clear as to what it means.

It is not clear how a word line can be coupled to first source/drain region of the transistors either.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 5, 6, 7, 8, 11, 12, 13, 14, 15, 18,19, 20 and 54, are rejected under 35 U.S.C. 102(e) as being anticipated by Yu US patent No. 6,268,253.

Regarding claim 1, Yu teaches a method of reducing a channel length in a transistor, comprising: forming a gate dielectric layer 204 on a semiconductor substrate 102; coupling a barrier layer 206 to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth; forming a gate 208 on top of the barrier layer, the gate

having sides, and an effective channel length defined by the sides; and oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide 212 and an effective channel length of the gate is reduced (figs. 4 and 5).

Yu does not explicitly state forming a barrier layer for preventing oxide undergrowth. Since silicon nitride is a well-known barrier layer, layer 206 inherently prevents oxide undergrowth.

Regarding claim 2, Yu teaches the entire claimed process of claim 1 above including coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer 206 to the gate dielectric layer 204 (fig. 4).

Regarding claims 5 and 6, Yu teaches the entire claimed process of claim 1 above including the gate dielectric layer on a semiconductor substrate comprises forming a gate oxide and gate dielectric layer 204 on a semiconductor substrate 102 (fig. 4).

Regarding claims 7, 8, 11, 12,13, 14, 15, 18, 19 and 20, Yu teaches the entire claimed process of claim 1 above including forming a first and second source/drain region 220 and 220 in a semiconductor substrate and forming a first source/drain extension 240 adjacent the first source/drain region and a second source/drain extension 242 adjacent the second source/drain region (figs. 6 and 7).

Regarding claim 54, Yu teaches the entire claimed process of claim 1 above including a transistor formed by the method of claim 7 (fig. 6).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 5, 9, 10, 16 and 17, in so far in compliance with 35 U.S.C 112 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Gardner et al. US patent No. 6,005,274.

Regarding claims 4, 5, 9, 10, 16 and 17, Yu teaches substantially the entire claimed process of claims 1 and 7 except explicitly stating that the coupling silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate layer to form a silicon nitride (SiN) layer.

Gardner teaches using remote plasma nitride process to form the gate barrier layer 16 (SiN).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate remote plasma nitride process taught by Gardner in the method of Yu in order to prevent the migration of undesirable elements from one region of the semiconductor device to other regions.

Claims 21, 22, 25, 26, 27, 28, 29, 32, 33 and 34, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu.

Regarding claims 21, 22, 25, 26, 27, 28, 29, 32, 33 and 34, Yu teaches substantially the entire claimed process of claims 1 and 7 except explicitly stating

forming a number of transistors on a semiconductor substrate and electrically connecting the number of transistors.

It is conventional to form more than one transistor and electrically connecting the transistors in a useful MOS device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make more than one transistor and connecting the transistors in order to form a semiconductor device that could be integrated in an IC chip.

Claims 23, 24, 30 and 31, in so far in compliance with 35 U.S.C 112 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Gardner et al. US patent No. 6,005,274.

Regarding claims 23, 24, 30 and 31, Yu teaches substantially the entire claimed process of claims 1, 7, 21, 27 and 28 except explicitly stating that the coupling silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate layer to form a silicon nitride (SiN) layer.

Gardner teaches using remote plasma nitride process to form the gate barrier layer 16 (SiN).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate remote plasma nitride process taught by Gardner in the method of Yu in order to prevent the migration of undesirable elements from one region of the semiconductor device to other regions.

Claims 35-48, in so far in compliance with 35 U.S.C 112 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Gardner et al. in further view of Sung et al. US patent No. 6,008,085.

Regarding claims 35-48, Yu teaches substantially the entire claimed process of claims 1 and 7 above except explicitly stating that the coupling silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate layer to form a silicon nitride (SiN) layer and forming a number of word lines coupled to the gates of the number of transistors; and forming a number of bit lines coupled to the first source/drain region of the number of transistors.

Gardner teaches using remote plasma nitride process to form the gate barrier layer 16 (SiN).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate remote plasma nitride process taught by Gardner in the method of Yu in order to prevent the migration of undesirable elements from one region of the semiconductor device to other regions.

Sung teaches word lines 10 coupled to the gates of the number of transistors; and forming a number of bit lines 26 coupled to the source/drain region of the number of transistors (fig. 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of forming a number word lines coupled to the gates of the transistors and forming a number of bit lines connected to the

source/drain region taught by Sung in the method of Yu and Gardner in order to integrate the semiconductor device with other part of an IC chip.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D and F are cited as being related to a MOSFET process.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Samuel Admassu Gebremariam
May 19, 2002

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800